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The Instrument Control Unit of the ESA-PLATO 2.0 mission

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ABSTRACT

PLATO 2.0 has been selected by ESA as the third medium-class Mission (M3) of the Cosmic Vision Program. Its Payload is conceived for the discovery of new transiting exoplanets on the disk of their parent stars and for the study of planetary system formation and evolution as well as to answer fundamental questions concerning the existence of other planetary systems like our own, including the presence of potentially habitable new worlds.
The PLATO Payload design is based on the adoption of four sets of short focal length telescopes having a large field of view in order to exploit a large sky coverage and to reach, at the same time, the needed photometry accuracy and signal-to-noise ratio (S/N) within a few tens of seconds of exposure time. The large amount of data produced by the telescope is collected and processed by means of the Payload's Data Processing System (DPS) composed by many processing electronics units.
This paper gives an overview of the PLATO 2.0 DPS, mainly focusing on the architecture and processing capabilities of its Instrument Control Unit (ICU), the electronic subsystem acting as the main interface between the Payload (P/L) and the Spacecraft (S/C).

Keywords: exoplanets detection, transit photometry, light curves, asteroseismology, ICU – Instrument Control Unit, data processing, data compression.

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1. INTRODUCTION

PLATO 2 [1] has been selected by ESA as the third medium-class Mission (M3) of the Cosmic Vision Program, to be launched in 2024. Its Payload is conceived for the study of planetary system formation and evolution and to answer fundamental questions about the presence and potential habitability of other planets similar to the Earth and planetary systems like our own Solar System.
Its baseline design, at the present time under review by the PLATO Consortium and ESA before Mission Adoption (foreseen for the end of 2016), is composed of 34 small telescopes whose fields of view will cover more than 2200 square degrees. The telescopes are split into two groups of 32 and 2 units. The latter will provide the capability to

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observe bright targets and are dubbed fast telescopes. Combined with the 32 (normal) telescopes, the whole set will make it possible to attain a large photometric visible magnitude range, from ~4 to ~16. Due to the present budget estimates for the mass and power consumption of the overall Payload, exceeding the ESA allocated resources, the present design is going through a likely descoping before Mission Adoption, in order to reduce the baseline number of telescopes and to fit the allocated budgets, but still preserving the scientific driving requirements and the Mission overall capabilities in terms of number of targets, photometric accuracy and achievable S/N ratio.

Focusing on a subset of brighter targets (m_v 4-11), the PLATO Payload will be able to detect and characterise planets down to Earth size by means of photometric transits, with their masses determined through ground-based radial velocity follow-up measurements. Moreover, given the brightness of this subset of samples, PLATO will extensively perform asteroseismology on these targets to obtain highly accurate stellar parameters as masses, radii and ages allowing for a precise characterisation of planetary bulk parameters.

The adoption of an observing program including two long pointing of 2-3 years each, will provide the capability to observe planets down to the habitable zone of solar-like stars with a first basic assessment of the main characteristics of their atmospheres, opening the way to future space missions designed to perform spectroscopy on these targets.

The main scientific requirement to detect and characterise a large number of terrestrial planets around bright stars plays a key role in defining the PLATO observing strategy and its own Payload.

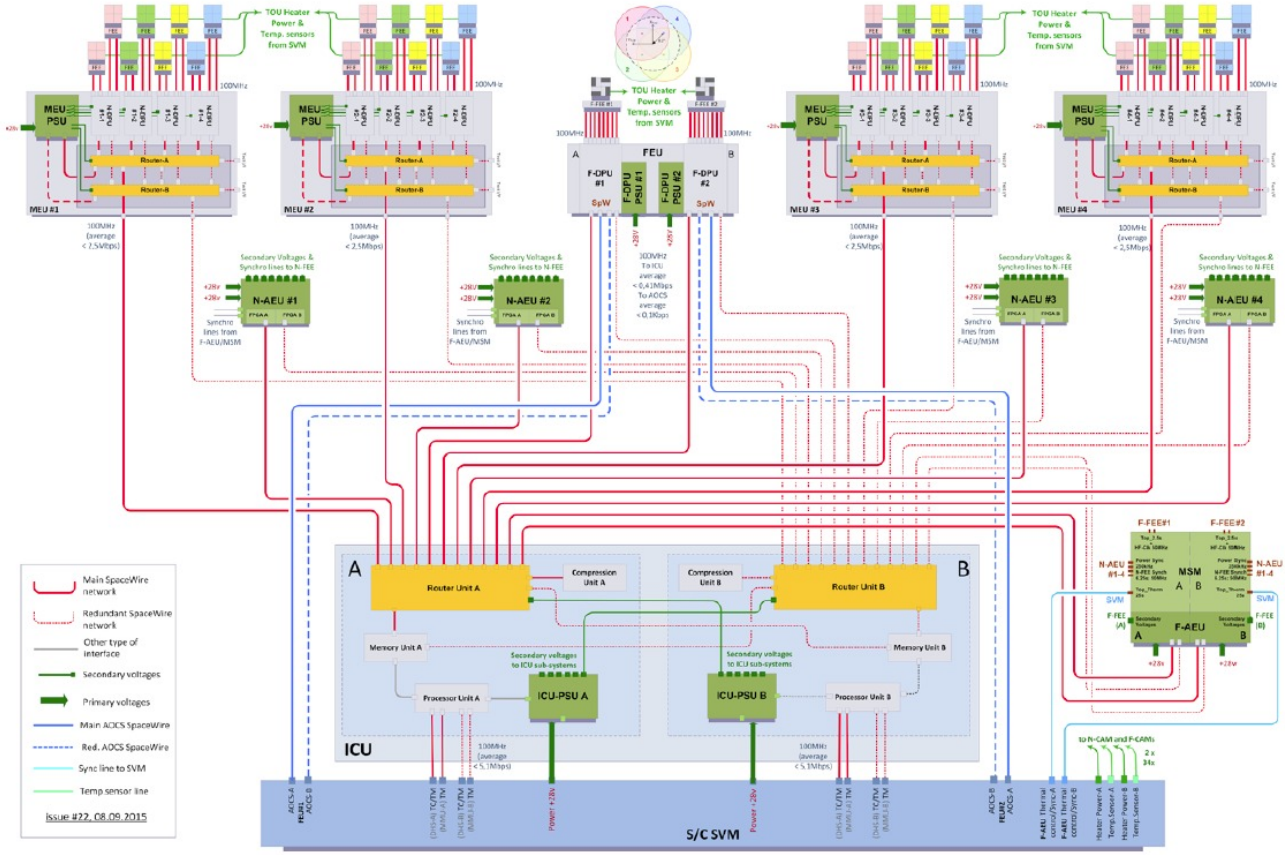

Figure 1: PLATO 2.0 Payload electrical architecture, showing the scientific data flow from the CCD focal planes (top) towards the ICU (bottom) and the S/C Service Module (SVM).

In particular, the 4 CCDs per focal plane, for a total of 136 CCDs, as baseline, pose strong constraints on the readout and the subsequent processing of a huge set of data, which requires then a customised Data Processing System (DPS).

The baseline DPS design is composed of 16 Normal DPUs (Data Processing Units) and 2 Fast DPUs (one per each Fast camera/telescope), refer to Figure 1, designed to pre-process the downloaded images and to extract the photometric signal

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from the selected targets as well as to select a reduced sample of imagettes of few pixels around a subset of stellar targets. The 16 DPUs, collected in groups of 4 inside 4 Main Electronics Units (MEUs), will also be in charge of the detection and removal of outliers from the photometric signals. All the scientific data and payload housekeepings will be collected by the Instrument Control Unit (ICU) [2] acting as the main interface between the Payload and the spacecraft. The PLATO ICU will be in charge of data collection from DPS and pre-processing, data compression, managing of the Payload SpaceWire network and received telecommands (TC), telemetry (TM) formatting towards the S/C. It is conceived as a full cold-redundant unit implementing a minimal cross-strapping to improve the overall DPS reliability.
This paper provides an overview of the overall PLATO 2.0 DPS, mainly focusing on the architecture and processing capabilities of the ICU, selected to fulfil the scientific and technological driving requirements of the Payload baseline design, hosting 32+2 telescopes. This will guarantee the Unit design suitability to address the overall processing requirements also in case of an instrument descoping, as required by the Mission Adoption by ESA.

2. ICU HW DESIGN DESCRIPTION

The present ICU design is implemented within a single unit internally redundant (Figure 2). Each chain is composed of 4 boards (plus a common backplane for signals routing) operating in cold redundancy:

- 1 Processor (CPU) board
- 1 Spacewire (SpW) Router & HW compression board
- 1 Mass Memory (MM) board
- 1 Power Supply (PS) board

The ICU baseline internal interfaces are shown in Figure 1. In particular a simplified ICU block diagram with the present adopted internal I/Fs, as designed by the ICU Team, is illustrated in Figure 2.

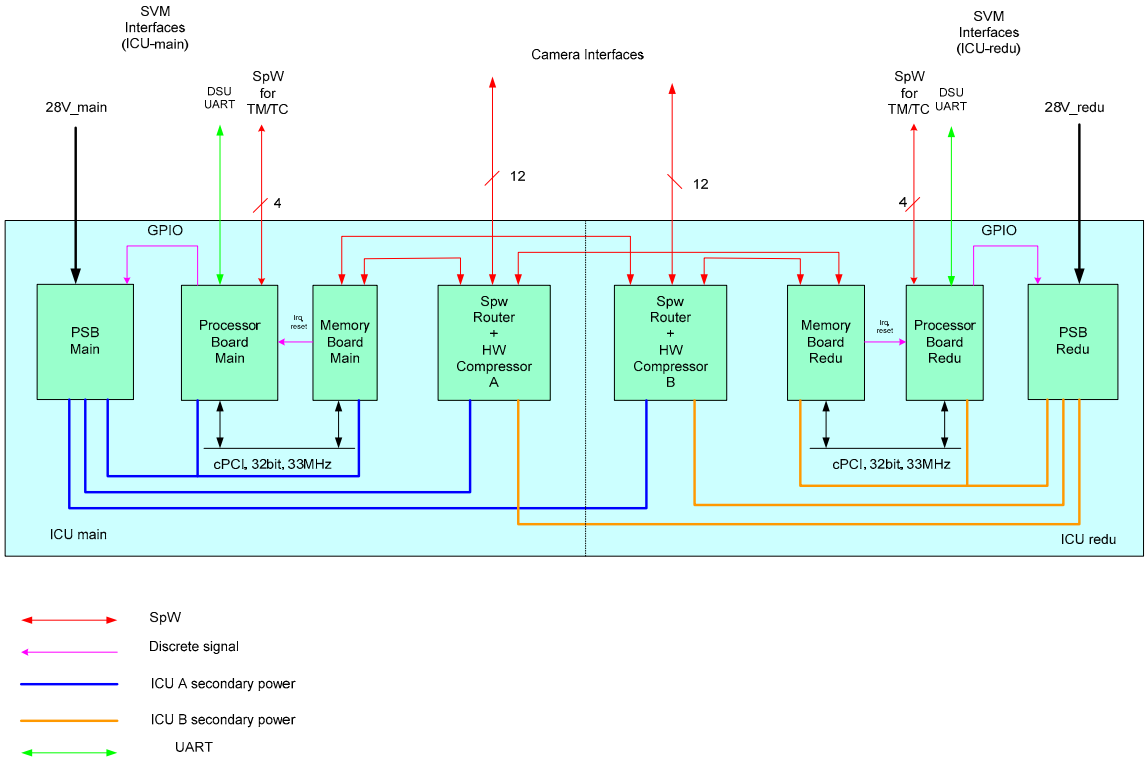

Figure 2: PLATO 2.0 ICU block diagram showing the baseline internal I/Fs.

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The two chains are interfaced by means of a common back panel. In particular the processor board and the memory board are interfaced thanks to a cPCI bus while both routers can be accessed via SpW links.
The ICU is switched on/off simply feeding the Power Supply line with the +28 V voltage as provided by the S/C, as the electrical interfaces toward the SVM do not exploit any HP/HV (High Power/High Voltage) command line as well as it is not foreseen any discrete line between P/L units.
The ICU I/Fs towards DPS are hereunder itemized:

ICU-DPS IFs:

- 12 SpW links (4 MEU + 2 F-DPU + 4 N-AEU + 2 F-AEU), as baseline

and towards the Service Module (SVM):

ICU-SVM IFs:

- 2 (M&R) TM SpW links to DHS
- 2 (M&R) TC SpW links to DHS
- 1 Power Supply line (+28 V)

The ICU mechanical design is illustrated in Figure 3, while the Unit mass budget is illustrated in Table 2 of the Budgets Section. The box is made of Aluminium alloy and its dimensions (including mounting feet) are 302 x 162 x 203 mm^3 (X x Y x Z), without considering connectors and bonding stud (allocated: max 293 x 260 x 251 mm^3, X x Y x Z, including mounting feet, connectors, and grounding lugs).

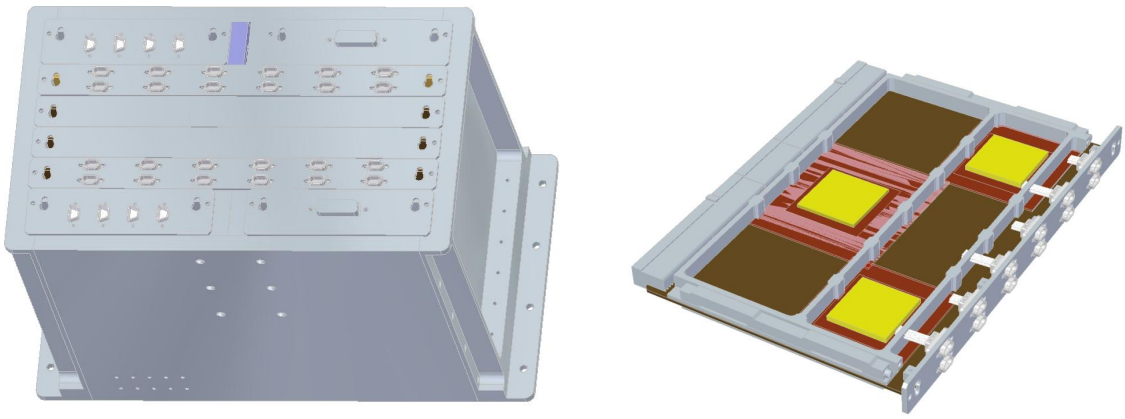

Figure 3: ICU box and boards arrangement with connectors on top the Unit as shown on the right for the case of the SpW router and Compression board.

The thickness of the lateral panels is designed to cope with the heat dissipation needs; in particular the thickness of the internal ribs improves the box strength and facilitate the heat sink. The unit fixing on the SVM optical bench is assured by means of two lateral lugs on the shortest sides of the unit, hosting 4 holes for M4 screws.
As baseline the Unit is composed of four nominal plus four redundant daughter-board modules perpendicularly plugged onto a back plane fixed by means of screws on the unit bottom plate (2 double boards in 6U format: Mass Memory and SpW Router boards plus 2 single boards in 3U format: CPU and Power Supply boards, as illustrated in Figure 3).
All the electronic boards are stiffened by a proper mechanical frame with the external I/O connectors fixed and screwed to the boards upper panels. The lateral sides of the modules are equipped with card-lock retainers that are used to fix the boards to the unit internal frame.

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The connectors arrangement exploits the Router board top panel on which 12 SpW customized connectors shall be located along the longest side as well as for the CPU and PS boards top panels. No external connectors are foreseen on the Mass Memory board top panel, located in the middle of the Unit (Figure 3).
The Unit adopts a 32 bit wide, 33 MHz, cPCI bus between the CPU board and the Mass Memory board and the SpW I/F between MM and SpW Router boards for TM/TC exchange. This configuration allows to cross-strap the SpW Router boards between Nominal and Redundant units adopting the power supply electrical scheme reported in Figure 6 to feed them.
The amount of SDRAM memories hosted by the Mass Memory board is 4 GB, as baseline, leaving about 40% of margin on the present expected data volume.

2.1 CPU board

The CPU board (Figure 4) shall implement, as baseline, the UT699 (LEON3FT) SPARC V8 microprocessor running at 66 MHz (or at 100 MHz, for the E version, as alternative solution) allowing up to 92 DMIPS, as required by the performed processing needs estimates and SVM I/Fs requirements. The processor will run the ASW on the RTEMS OS. One of the main characteristics of the UT699 CPU is the on-board availability of 4 embedded SpW links (2 supporting RMAP - Remote Memory Access Protocol, not available on the LEON2 CPU adopted up to the end of the previous Phase A) allowing to be directly interfaced to the SVM without the need of a SpW router as we foresaw during the Assessment Phase design.

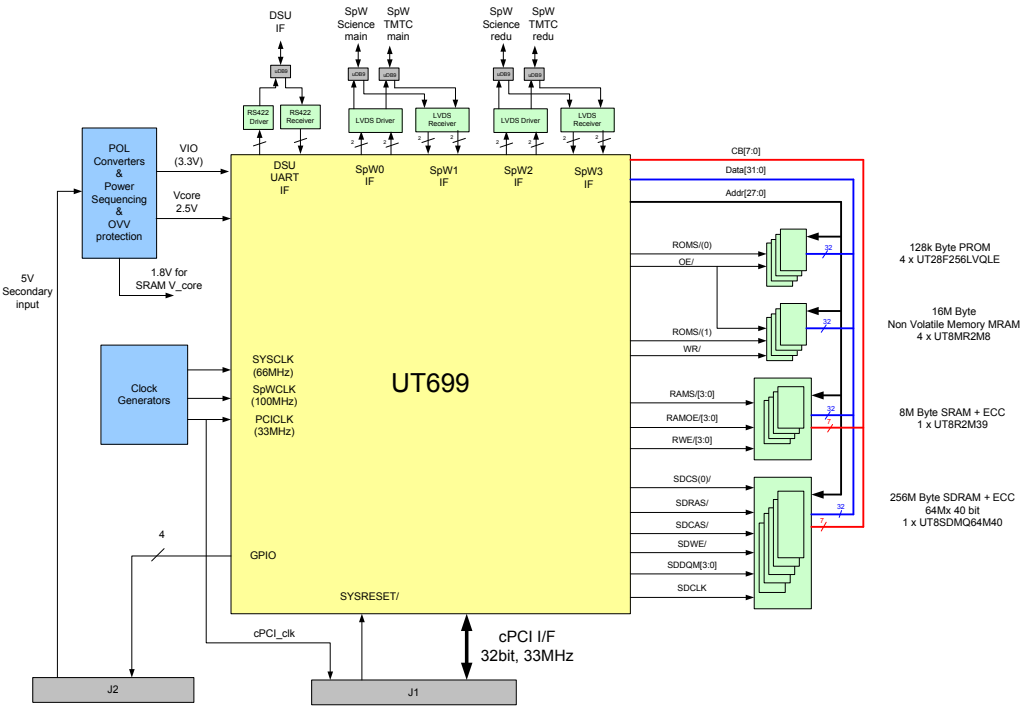

Figure 4: CPU board block diagram.

The processor includes an on-chip Integer Unit (IU), a Floating Point Unit (FPU), a Memory Controller and a DMA (Direct Memory Access) Arbiter and a DSU (Debug Support Unit) I/F. It is interfaced to the Mass Memory board by means of a 32 bit wide, 33 MHz, cPCI bus supporting DMA and hosting the controller and EDAC (Error Detection And Correction) capabilities for the memories, directly interfaced to the CPU. In this way, fault tolerance can be supported using EDAC on the external data bus.

The memories managed by the CPU are basically of three types:

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1) the non-volatile memories as the 128 KB PROM for the boot SW and the MRAM memory (32-bits access, capacity of 16 MB + internal ECC) hosting the ICU and N/F-DPUs images of the Application SW (ASW) and the stars catalogue;
2) the SRAM memory allocated to the software execution and local data processing (8 MB as baseline) and
3) the SDRAM memory (256 MB, as baseline) for the CPU data retrieval, processing and local buffering, as shown in Figure 4.

The on/off switching of the CPU board is achieved by switching on/off the related DC/DC converter module inside the Power Supply board. This happens when the SVM switches on/off the Nominal or Redundant +28 V lines.

The ICU ASW, running on the CPU, is the main software managing several interfaces and implementing the standard PUS – Packets Utilization Services but also a set of services specific to the PLATO 2.0 mission. The ICU ASW is responsible for managing also the payload modes. These include: switching on/off, configuring and commanding the DPS sub-units, verifying and executing the telecommands received from the S/C, monitoring the ICU and DPS sub-units, reporting housekeepings and events, supporting the FDIR (Fault Detection, Isolation and Recovery) capability; managing the local on-board time through a combination of the absolute time (received from the S/C through the SpaceWire protocol and Time Codes) and the internal time (based on a ICU HW clock); distributing the local time to the DPU boards as well as processing, compressing and packetizing some of the entries data sent by the DPS.
The ICU ASW shall communicate with the spacecraft using the CCSDS protocol over the SpaceWire link: the timestamp written in the packets will be based on the local on-board time.
A viable alternative for the UT699 and UT699/E could be represented by the new UT700 processor running at 166 MHz CPU (230 DMIPS - high computing capabilities) but with the uncertainties connected to a low heritage and the space-grade device availability, differently from the UT699/E, which is a mature device (QML-V grade).

ICU Remote Memory Access Protocol capabilities

In the context of the PLATO 2.0 mission, studies are going on in order to refine the concept of a RMAP bootloader for the Normal and Fast DPUs ASW. With the large number of DPU boards making up the on-board data processing system, the benefits could be huge for the PLATO Payload.
The N-DPU boards are presently based on the Dual Core GR712 (running at 100 MHz) and on a RTAX4000 FPGA. The latter communicates with the ICU over the SpW Router hosted by MEU. It uses a FPGA embedded SpW router and 4 RMAP IP cores interfaced to a memory controller by means of an AMBA AHB bridge. In this way memories and registers internal to the N-DPU boards could be configured, read and written by means of the standard RMAP SpW-compliant protocol.
The ICU and N/F-DPUs Application Software shall be stored inside the ICU CPU board NVM (MRAM based). The ICU shall also manage the maintenance of both the ICU and DPU application SW. With this approach, the DPUs boot process can be based upon the RMAP protocol: no PROMs/E2PROMs hosting the boot SW (criticality level B, according to the ECSS-E-40 - SW Engineering Standard document) and the ASW are needed at DPU level in this case (full hardware boot), but an adequate sized NVM shall be implemented only at ICU level.
The boot process of each DPU ASW will be performed remotely, over the SpaceWire link, by means of the ICU CPU exploiting the RMAP protocol (TBC by further analysis and tests, but the GR712 normally support this capability). Each N-DPU board will integrate a RMAP HW controller, which allows the ICU to access any area of its memory, including the processor registers. The RMAP protocol offers all the mechanisms allowing a high reliability for the remote memory write and read operations. In this sense, the RMAP protocol is very suitable for implementing a remote boot mechanism for the DPUs flight software.
Thanks to the RMAP protocol, the ICU can remotely configure the registers of the processor inside the DPU boards, loading a software image into the SRAM and starting it without intervention of any local boot software. In this way, the boot process of the DPU software is entirely under the responsibility of the ICU application software.
Indeed, the actual need of a small PROM aboard the N/F-DPUs (or MEU) with minimal characteristics for storing some permanent SW parameters needed to boot the basic HW will be further analyzed in the next phase.
It is worth noting that the ICU is the only DPS unit acting as a master so, in principle, the RMAP protocol could be directly managed by SW by means of the CPU UT699. In this way no RMAP SpW IP core would be necessary on the MM board, leaving more FPGA resources for other control and processing tasks. The RMAP core acts as links initiator managing in HW only a part of the RMAP protocol. This capability allow to perform CRC checks on telecommands as

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well as the transmission of linked commands list and to receive reply packets formatted in a structure capable of managing the detected errors in independent status words.
The pure SW RMAP protocol management would require more CPU resources and, given the present margins, it is preferred to have a mixed SW/HW implementation exploiting the RMAP cores inside the MM FPGA (refer to paragraph 2.2). Further studies on this topic will be performed during the next phase.

2.2 Mass memory board

The Mass Memory board (Figure 5) is based on a FPGA (RTAX2000, as baseline, implementing as HDL (HW Description Language) core an ECC (Error Correction Circuit) autonomous scrubbing engine with a SECDED embedded circuit used for SDRAM scrubbing) acting as the main memory controller, able to manage 4 GB of Synchronous Dynamic RAM (SDRAM) implemented with 3D-Plus memory cubes, as baseline. These radiation-tolerant memory stacks cubes enable high density and high-speed data transfer solutions, using modules with capacities from 1 to 4 Gb.
The MM board FPGA is interfaced to the CPU board by means of a 32 bits wide cPCI bus running at 33 MHz with Direct Memory Access (DMA) capabilities, while the bus towards the memories blocks is 40 bits wide (32+8 bits for EDAC function). The 32 bits wide cPCI bus, running at 33 MHz, provides a Unit internal theoretical data rate (bitrate) of 132 MB per second (1056 Mbps).

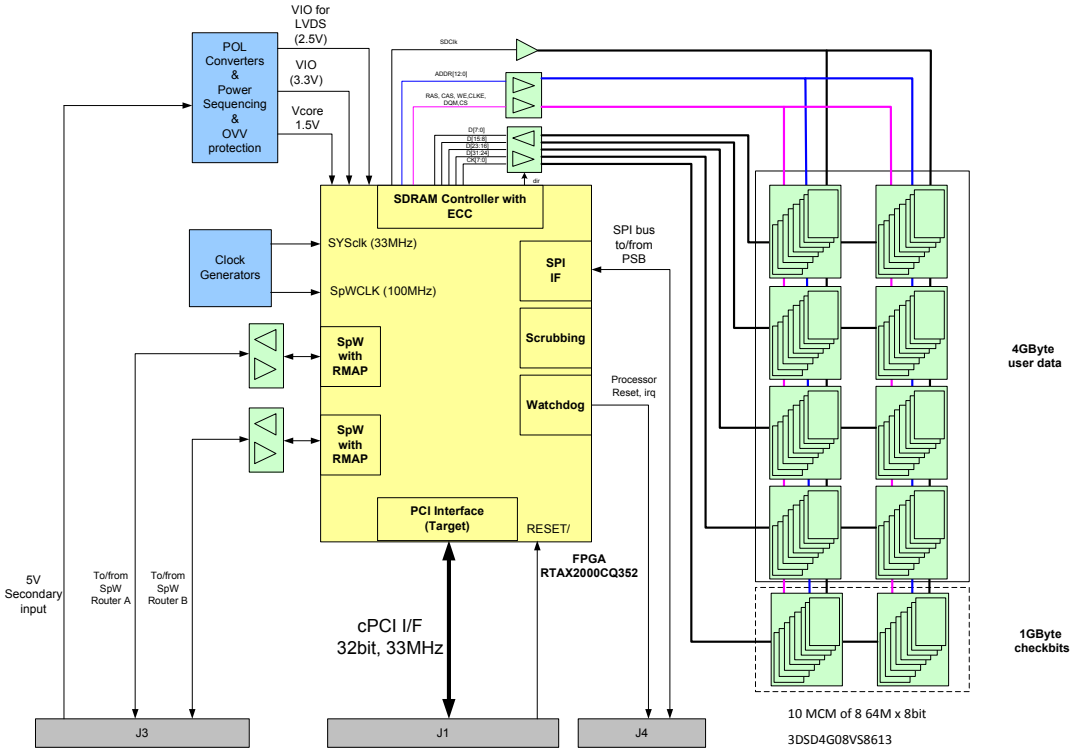

Figure 5: Memory board block diagram.

The times needed to access the SDRAM memories (write, read and refresh operations) are based on the characteristics of the adopted memory and the access operations to the memory itself will be managed by the ASW scheduler (e.g., static in time-multiplexing mode). The latter is not yet defined and it is too early to assess the bus accessing/timing scenario and how the CPU processing load could be affected by it. Anyway, given the theoretical bus speed, the design foresees enough margins for the time needed for buffering, at least for the data-reception operations.
From the functional point of view the memory area is basically partitioned in sectors, being the sector the minimum area that can be allocated by the SW file manager function to a file/packet store.

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The sector size is an important parameter to be set during the early design phase as compromise between the memory granularity and the required I/O throughput. As a matter of fact, the smaller the sector, the higher is the rate of the interrupts to be managed by the controller module during the storage and retrieval operations. As baseline we consider a sector size of 1 Mbyte and memory words of 4 bytes. The adoption of the DMA capability will limit the CPU interrupts release rate and the overall interrupts management complexity.
The ICU proposed for PLATO 2.0 hosts 2 fully independent Mass Memory boards (1 operating and 1 cold back-up), each providing a net usable memory capacity up to 4 Gbytes as baseline but they can also be provided with options hosting respectively 2 and 6 Gbytes of memory capacity. The overall ICU power consumption strictly depends on the adopted amount of memory and its actual use. For the next design phase it is foreseen a deeper study concerning the possibility to further reduce the overall memory needs to 2 GB allowing for a reduction of the overall Unit and Payload power consumption, as required by the ESA allocated budgets.

2.3 Power supply board

The Power supply board (Figure 6) is based on DC/DC converters and consists of three sections:

- Power conditioning section with:
  - Inrush current limitation;
  - Polarity inversion protection;
  - Power-on sequence generation;
  - Unit power-on reset generation;
  - EMI (Electro-Magnetic Interference) filtering;
  - DC/DC conversion with 3 independent DC/DCs: main DC/DC for the generation of the +5 V to be distributed to the other boards, Aux DC/DC for internal logic powering, HK DC/DC for powering the HK section for acquisition of voltages/currents/temperatures housekeeping.
- Power distribution section with four built-in Output Power Controllers (OPC), implementing overcurrent and overvoltage protection functionalities;
- HK acquisition section with 12 bits analog to digital conversion controlled by the processor via SPI bus (voltages and currents measurements).

On the power supply board it is also foreseen the acquisition of AD590-type temperature sensors (refer to HK section on Figure 6). The TRP (Temperature Reference Point) sensor will be located on the expected hot spot of the unit in order to provide the temperature values in telemetry.
Each PSB can provide power to both the SpW Router boards. Which router is going to be powered (N or R) is controlled by the Processor board via discrete commands (CPU GPIO - General Purpose IO port).
Each electronic board owning to the ICU is basically supplied by a main voltage level of +5 V protected for overvoltage and overcurrent and locally are derived the secondary voltage levels needed by the hosted electronic components by means of a so-called Point of Load.
The ICU is responsible for acquiring its own secondary voltages levels and current consumptions and shall also collect and transmit the HK data coming from the other subsystems. The monitoring of the voltages and current levels of the main lines (+5 V) as well as the monitoring of a TBD number of temperature sensors will be performed on board the HKs Acquisition Section, while each OPC will integrates the OVP/OCP functionalities (overvoltage/overcurrent protections).
The MEU-PSUs (Main Electronics Unit-Power Supply Units), hosted by the DPS, are responsible for the acquisition of the voltage levels and current consumptions of the four MEUs (voltage levels and current consumptions of each N-DPU board and of the router units). The analog-to-digital converted data shall be collected by the ICU thanks to the SpW network.
Each fast or normal DPU shall receive the CCDs and camera analog HKs (temperatures and voltage levels) from the FEEs. These analog HKs shall be transmitted to the ICU through the SpW network, once locally converted to digital values.

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The Fast DPUs, the AEUs (Ancillary Electronics Units) and the F-AEUs are responsible for acquiring their own voltage levels and current consumption. Also these HKs shall be sent to the ICU through the SpW network.
It is not foreseen the monitoring of the primary voltages and current levels feeding the Power supply board as it is assumed that this kind of measurement is directly provided by the SVM.

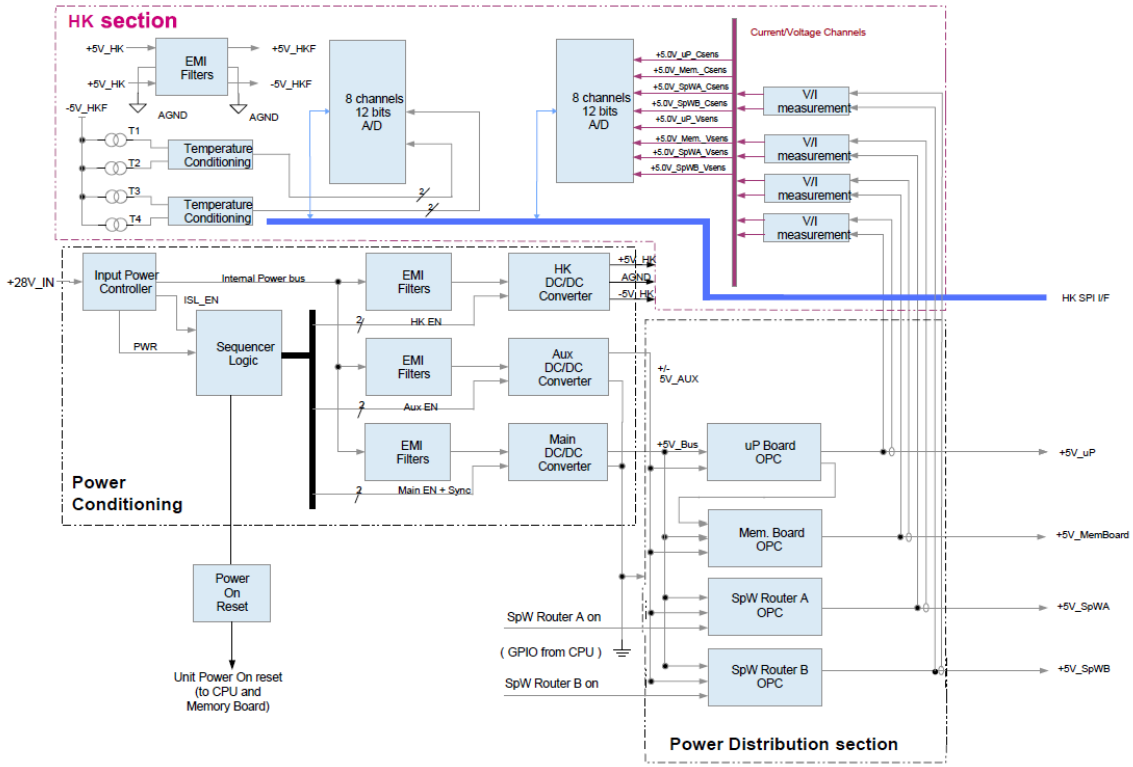

Figure 6: Power board block diagram.

The main DC/DC converter complies, as baseline, with the following specifications:

- Nominal load voltage: +5.0 V
- Maximum output current: 10.0 A
- Input voltage: 16.0 ÷ 40.0 V
- Efficiency @ Vin = 28V: 78%
- Efficiency @ Vin = 16V: 80%
- Efficiency @ Vin = 40V: 75%

2.4 SpaceWire router and HW compressor board

The overall data processing including compression of the scientific data (fluxes, centroids and 6x6 pixels imagettes) performed, as an estimate, with a LEON2 FT running at 100 MHz, is critical when processing 2k imagettes/camera (only compression) and impossible at the present time with 12k imagettes/camera, as required following the satellite Ka-band transponder adoption, allowing for a larger data rate towards Ground with respect to previous considered X-band transponder.
Even considering more performing LEON-based products, like the UT699/E, the full compression in SW has been demonstrated not feasible. The introduction of an FPGA-based HW compression engine to be used as baseline for the imagettes only will reduce the computational power required by the CPU.

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The main function to be implemented on the HW compressor module is the Rice (CCSDS 121.0) lossless compression. The HW-implemented algorithm shall be parameterizable (with parameters TBD) and at least a compression ratio (CR) of 2 shall be reached. Data types to be managed by the HW compressor module are integers (16 bits depth pixels).
In the simplified block diagram illustrated in Figure 7, imagettes coming from the SpW network are routed to the Mass Memory board and, from memories, to the HW compressor engine that performs the compression and stores the compressed data in a SRAM or DRAM buffer. The processor can retrieve the compressed imagettes data and write them in the required science data packet for TM, towards the SVM.

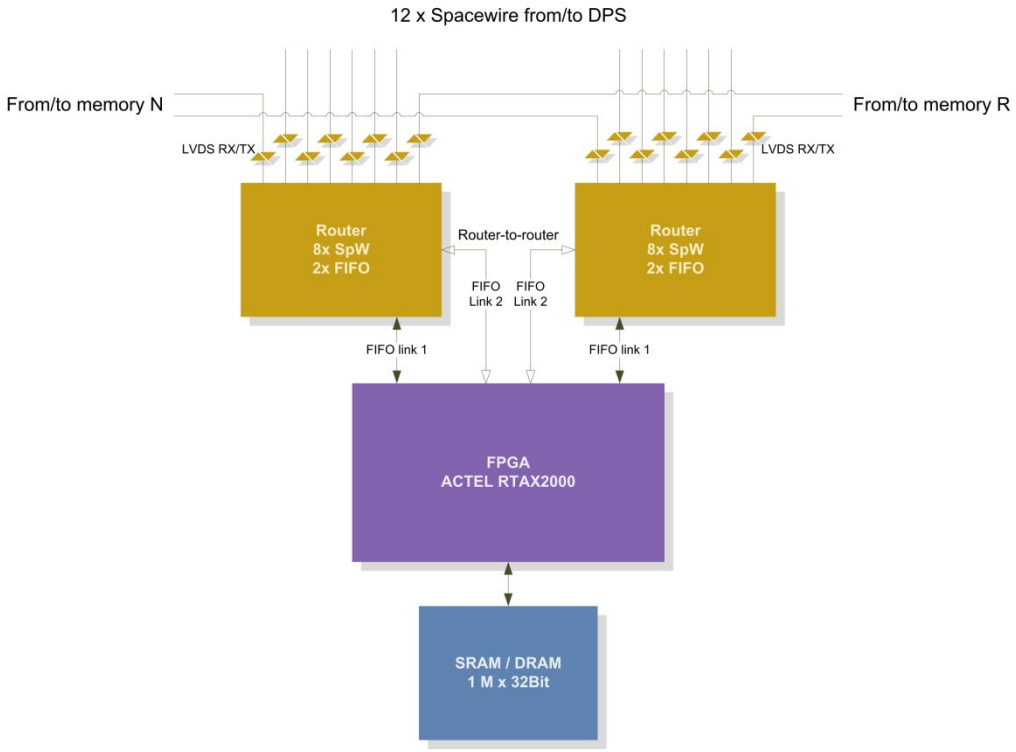

Figure 7: SpW Router and HW compressor board block diagram. The HW compressor core is implemented inside the control FPGA.

The SpW router & HW compression board includes as baseline four subsystems:

- A SpW Router section with 12 external SpW links towards DPS and 2 SpW I/Fs towards N and R Mass Memory boards;
- An internal SpW or FIFO link between the adopted routers;
- 14 or 16 SpW drivers/receivers (no transceivers are used for the link between the two routers);
- 4 Mbytes of SRAM/DRAM-type memory for buffering and supporting the local processing;
- An ACTEL RTAX2000 FPGA, whose test functionalities and properties (Figure 8) are hereunder itemized:
  - Functional Test
    - Link connection set-up, protocol for single link
    - Physical performance (100 Mbit) for one link
    - Protocol for multi-link transfer
  - Router-to-Router (redundancy)
    - A: via Spacewire or
    - B: via FIFO Interface (loop through FPGA)
  - Time Synchronization
    - Time transfer from PC through RDCU (Router and Data Compression Unit) to DPU-simulator
  - Performance Test

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- Multilink performance
- Performance of compression unit
- Performance with maximum data rates (DPU's and compressor)

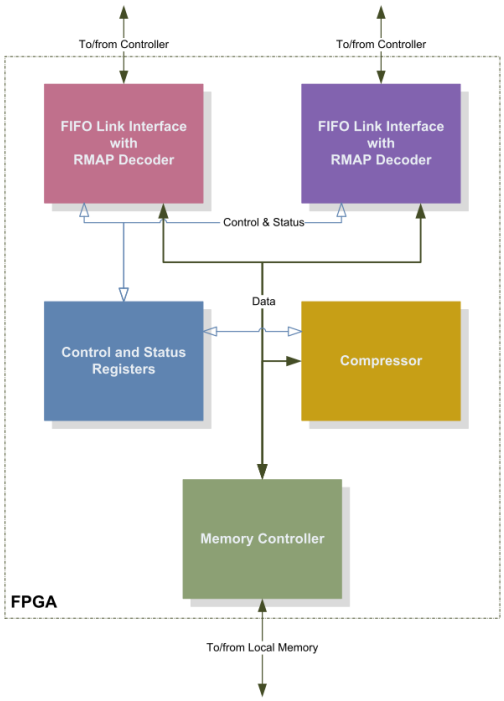

Figure 8: SpW Router FPGA block diagram with basic HW cores and their functionalities.

2.5 Backplane

The backplane hosts the internal connectors to plug all the ICU boards, acting as a routing board for power, digital and analog signals. It represents the mean through which the Nominal and Redundant daughter-boards are connected and share the power and signal lines each other. Thanks to the use of a backplane all the I/O connectors are directly mounted on the relevant PCB modules and there are no wired connections, as baseline, inside the unit.
The backplane is equipped with straight connectors and lies on the unit bottom panel while the daughter-boards are inserted through the top of the unit and plugged onto the same backplane through linear connectors. All the daughter boards are fixed to the ICU box mechanical frame by means of card lock retainers.
In order to limit likely digital to analog crosstalk noise effects between connectors and power/signal lines the baseline backplane design adopts cPCI connectors available from Hypertac procured according to NASA GSFC S-311-P-822 specification and already adopted on EUCLID DPU/DCU and CDPU units. The cPCI 32-bit bus will be routed between processor and mass memory on P1 connector following as guideline the cPCI specifications.

3. BUDGETS

The present power and mass budgets for the updated design, as required by the ICU higher-level requirements, are those reported in Table 1 and Table 2. In particular, Table 1 shows the power budget for an optional solution too, hosting 2 GB of memory on the MM board. This solution could be viable in principle because the previous assumption to perform on board the ICU the outliers detection and removal led to an increase of the needed memory. Devolving this kind of processing to the N-DPUs as well as assuming a reduced Design Maturity Margin (DMM, 20% presently) during the

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next Phases could reserve a potential reduction of the ICU actual need of buffering up-to 2 GB max, leading to a meaningful saving in power (about 4-5 W).
The ICU power consumption strongly depends on the actual I/O throughput it shall sustain as well as on the mass memory size. A more detailed estimate of the maximum power consumption will be computed during the ICU Avionic Model development and testing (B2 Advanced and B2 Phases) once the above parameters will be definitely fixed (CPU clock, effective memory use, I/O throughput, etc.).

Power Budget						
Options	CBE	DMM 20%	MEV	MPV[1]	Margin	Margin
	W	W	W	W	W	%
Baseline 4 GB	30.94	6.19	37.12	30.3	-6.82	-22.5
Option 2 GB	27.44	5.49	32.92	30.3	-2.62	-8.6

Table 1: ICU Power Budget (CBE: Current Best Estimate; DMM: Design Maturity Margin; MEV: Maximum Expected Value; MPV: Allocation or Maximum Possible Value).

Also the present ICU mechanical design shows room for further optimization and mass saving recovery actions shall be taken into account in the next phase of the project to come closer to the applicable ESA mass target.

Mass Budget						
Options	CBE	DMM 20%	MEV	MPV	Margin	Margin
	Kg	Kg	Kg	Kg	Kg	%
Baseline 4 GB	7.570	1.514	9.084	7.800	-1.284	-16%

Table 2: ICU Mass Budget (CBE: Current Best Estimate; DMM: Design Maturity Margin; MEV: Maximum Expected Value; MPV: Allocation or Maximum Possible Value).

4. ICU SW DESIGN DESCRIPTION

The ICU OBSW is composed of two different parts: the Boot SW (BSW) and the Application SW (ASW). The latter includes also the Compression SW (CSW), in charge of the University of Wien.

4.1 Boot SW

The BSW starts its execution once the unit is switched on: the development of this code is under responsibility of the industry manufacturing the unit.
The tasks performed by the BSW are mainly:

- Check of the integrity of the hardware;
- Initialization of communications with the service module (SVM);

[1]The MPV of the average (over 25 seconds) maximum primary power consumed and dissipated by the ICU, including all design maturity margins, shall be lower than 30,3W as indicated in the ICU User Requirement Specification (URS) document.

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- Waiting for telecommands, either to launch the ASW (copy of the selected SW image from the Non Volatile Memory – NVM to Program Memory – PM and jump to the code) or to upload a new ASW image.

In principle, it is possible to start the communications with the DPUs already at this stage but we strongly supports the scenario in which the BSW tasks are limited to the internal ICU handling, while all the other tasks are under ASW control. In this way, it is possible to define the interaction between the ICU and the DPUs at a later stage, and to leave margins to change the communications protocol during the whole instrument development lifecycle.
The BSW is stored in a permanent non-volatile memory (PROM): the first step to run this SW is then to copy it from PROM to Program Memory. This step is usually performed by means of a HW based finite state machine residing inside a FPGA or directly by the CPU. Once the BSW starts, the HW, e.g., the interface with the satellite, is initialized.
The first tasks of the BSW, executed autonomously, are the memory checks: RAM (all the memory units) and NVM (MRAM, via checksum). If one or more errors are found the BSW generates a report sent to the satellite with an event packet, typically a (5,4) packet (of the Packet Utilization Standard – PUS Services). In any case, the switch-on sequence continues.
After the NVM check, if the memory report is OK an event packet (5,1) is sent to the satellite and the BSW waits for a telecommand. At this stage, three kinds of commands are expected: boot from NVM; a set of memory load commands to upload a new ASW; start the ASW. If the ICU receives another, unexpected, command the BSW reacts with a (1,2) packet specifying the not valid Type and/or Subtype.
The Boot from NVM command copies the content of the NVM in PM (in case two or more images are available this command specifies the ID of the image to execute); afterwards, the checksum is computed to ensure the integrity of the copied image. If the procedure succeeds the ICU waits for the command to start the ASW (this last step is probably not necessary because the ASW can be started immediately after the copy is successfully executed).
To upload a new image a set of memory management commands are sent to the ICU: each command contains a portion of the ASW, which is copied to the address given in the packet. A checksum is computed before and after the copy. Once the whole image has been received, the ASW can be started.
Finally, when the ASW is ready for execution, either after the copy from NVM, or after a complete upload, the command *Start ASW* can be sent: on reception of it, the BSW makes some final operations, if necessary, and then make a jump to the location in PM where the ASW begins.

4.2 Application SW

In the next figure we show a logical model of the application software (ASW). It is meant to represent in a graphical way the functionalities of the SW and the flow of data.
The telecommands from the satellite are examined by the *TC receiver* module making all the foreseen checks (APID, length, CRC, etc.). The positive or negative acknowledgment is sent to the *TM handler* that controls the data flow to the satellite. The telecommands are then sent to the *Controller* that interprets the content: if the command is for a subsystem, it is sent to the *SubSysTx1* module that relays the command to that unit. The subsystem receives the command and reports back an acknowledgment (ACK), either positive or negative. A negative ACK triggers a reaction on the ICU side, according to the Autonomy Functions (AF) library.
If the command is for the ICU, the Controller executes it. The commands can be:

- handling of the memory (load, dump, check);
- handling of the instrument operative modes (observing and calibration modes etc.);
- upgrade of the ICU tables (list of stars, library of the AFs, science data processing parameters, and so on);
- on-board time management;
- telemetry control (enabling/disabling packets transmission);
- housekeepings (HK) management (e.g., upgrade of validity interval);
- additional services (e.g., *Are-you-alive* service).

The *HK Handler* module generates the ICU internal data and receives the data from the subsystems: the values are checked against an internal list and any out-of-limit condition is signaled through event packets and, if defined, an AF is triggered. A periodic packet reports the last HK values.
Science data received from the DPUs are transferred to the *Science data manager*: on the base of the data type, they are sent to the *HW compressor* module or to the *Science data processing* module. The former is designed to compress the

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imagettes; the compressed data are then sent to the TM handler. The latter module compresses the fluxes and the centroids (it is also possible that they will be compressed by the HW compressor too), or performs other kind of analysis. The ASW will have an internal reference time based on the CPU board HW clock. This time will be synchronized with the absolute time provided by the satellite by mean of specific telecommands. The time information will be used mainly inside the TM handler that writes the time stamp in the telemetry packets. It will also be distributed to the DPUs.

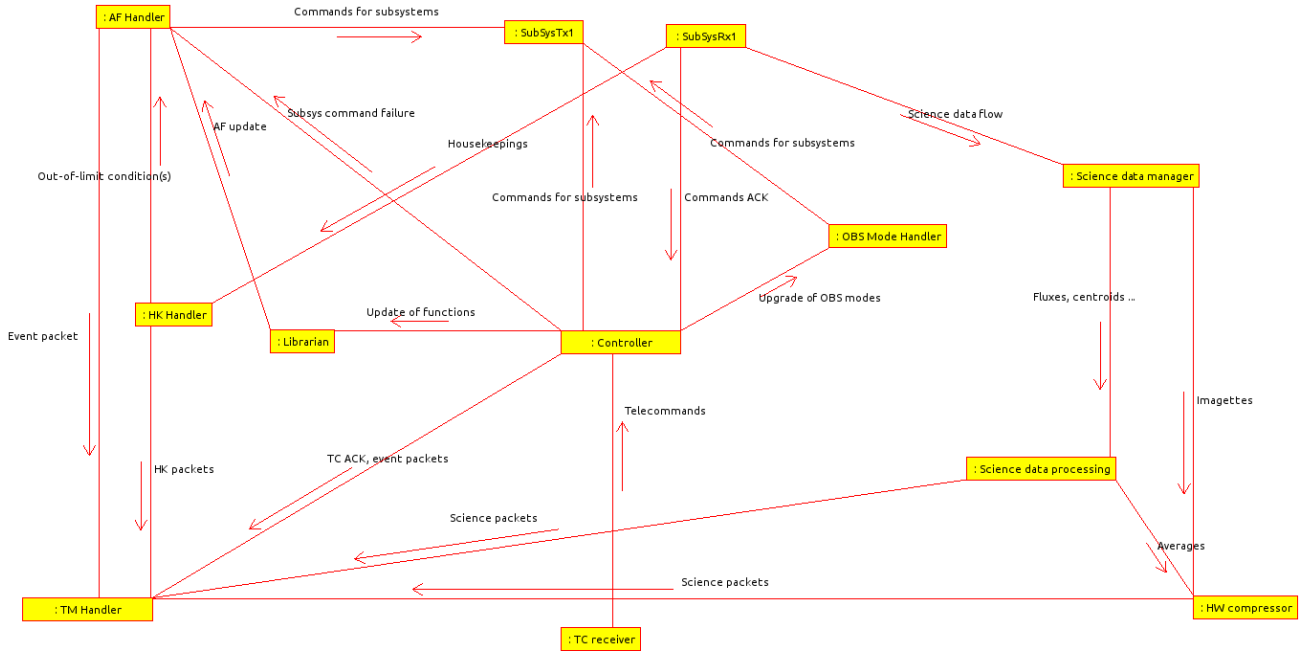

Figure 9: ASW logical model.

4.3 FDIR design

An important issue to be addressed is the FDIR (Failure Detection, Isolation and Recovery): at this stage of the ICU development, with the HW design not yet finalized, it is not possible to go deep in the FDIR philosophy. A general concept can however, be presented: a first case of failure is a SW failure (bit flip) in memory, which is solved by EDAC in case of a single event. More complex cases are difficult to be found, or even impossible, but are very unlikely to occur. In case of such a failure the ASW will generate an event (5,1) for a single bit flip; more general cases will be considered further on.

HW failures (e.g. the physical damage of a memory cell) can be discovered through periodic memory checks. These can be done autonomously by the ASW, or requested through telecommands. The area that can be checked is mainly the zone containing the program code since the areas that contain data have a content that cannot be known a priori, so a memory check is unfeasible. In case of broken/corrupted cells in the program memory area, the solution will be trying to relocate the code: this operation depends on many details which are not known at present but as long as possible the ASW will be designed keeping in mind this possibility. Other possible failures are in the non-volatile memory, which contains the images of the SW (of the ICU and of the DPUs): again, this occurrence can be detected through periodic memory checks. Likely, this memory will be written in pages, so that once a failure is found, the specific page will be discarded. This recovery procedure clearly works as long as free pages are available.

For the PLATO 2.0 mission, which is characterized by a high TM rate, an important aspect is the handling of the data rate, both from DPUs to ICU and from ICU to SVM, especially during the SW development and instrument integration. So the filling of the buffers will be monitored and in case events will be generated: the buffer that receives data from the DPUs will be a circular buffer with the filling factor configurable via SW, e.g. signaling when the buffer is full at 50% or 75%. The special (and catastrophic case) of buffer full at 100% is expected to happen only during testing activities and will be handled with dedicated functions. Concerning a possible SW failure leading to a “frozen” ICU, it is foreseen to be handled with the use of a watchdog that will reset the unit.

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Another important aspect of FDIR is the check of the HW housekeepings: those that must be checked will have defined an interval of in-range limits. If an HK goes out-of-limit the ICU will issue an event (5,x), depending on the severity of the failure, and, if defined on ground, an autonomous function will be executed.
Also the switching between nominal and redundant sections of the unit will be an important part of the FDIR. When there is a cold redundancy, which implies a switch from the whole nominal unit to the whole redundant unit, such a switch is an easy task handled by the spacecraft that, simply, switches off the nominal unit and gives power to the redundant one.
In our case, on the contrary, the presence of a (minimal) cross-strapping between the nominal and redundant sections of the unit makes it quite tricky the switch from (part of) one section to (part of) the other section. Specific test will be designed and executed once the first nominal + redundant units will be available on the Unit Engineering Model (EM).

5. CONCLUSIONS

In this paper we have provided an overview of the current design status (May 2016) of the Instrument Control Unit of the PLATO 2.0 Mission, as derived from the relevant requirements specifications, contained in the overall PLATO Consortium documentation. The presented electronics and SW designs have been redacted thanks to the contributions provided by INAF with OHB/CGS Italy, University of Wien and the Space Research Institute (IWF, Graz) of the Austrian Academy of Science.

Until the end of the next B2 Phase a more detailed study, supported by laboratory testing activities on the ICU commercial breadboard and on the Avionic Model (as foreseen by the Unit Model Philosophy) shall be conducted with the contribution of the on-going selection industrial partner (ICU Prime), in order to address all the PLATO 2.0 Payload scientific and technological requirements. The latter, as well as the updated ICU design, will be reviewed up to the Mission Adoption and consolidated thanks to the next project milestone, the Instrument Preliminary Design Review (IPDR).

6. ACKNOWLEDGMENT

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Finally, we would like to thank OHB/CGS Italy for the continuous and precious support in refining the present ICU design as well as the industrial programmatic aspects during the preliminary and detailed design definition phases of the PLATO 2.0 Mission, selected in the framework of the ESA's Cosmic Vision Program 2015-2025.

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